

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 – 8 (Canceled)

- Claim 9. (Previously Presented) A method of fabricating a multi-layer lithographic semiconductor, comprising:
- applying a first resist layer to a semiconductor substrate;
 - masking said first resist layer and exposing said first resist layer, thereby forming a first latent image in said first resist layer;
 - adding an opaque barrier layer to said first resist layer covering said first latent image;
 - applying a second resist layer to said opaque barrier layer;
 - masking said second resist layer and exposing said second resist layer, thereby forming a second latent image in said second resist layer;
 - removing said second latent image;
 - etching said opaque barrier layer; and
 - removing said first latent image.
- Claim 10. (Original) The method of claim 9, further comprising preparing said substrate.
- Claim 11. (Original) The method of claim 9, further comprising applying post-application resist treatments.
- Claim 12. (Original) The method of claim 11, wherein said post-application resist treatments are selected from at least one of the group consisting of: softbake, hydration, and ammonia based image reversal.

- Claim 13. (Original) The method of claim 9, wherein a shape of said first latent image and the second latent image is selected from the group consisting of: square, rectangle, triangle, circle, oval, and polygon.
- Claim 14. (Original) The method of claim 9, wherein said etching is selected from the group consisting of wet etch, dry etch and develop/exposure.
- Claim 15. (Original) The method of claim 9, wherein said exposing uses rays selected from at least one of the group consisting of ultraviolet light, electrons, and x-rays.
- Claim 16. (Original) The method of claim 9, further comprising using alignment tools.
- Claim 17. (Previously Presented) The method of claim 9, further comprising adding a second opaque barrier layer on said second resist layer, applying a third resist layer on said second opaque barrier layer, masking said third resist layer and exposing said third resist layer, thereby forming a third latent image in said third resist layer, removing said third latent image, etching said second opaque barrier layer, and removing said second latent image.
- Claim 18. (Previously Presented) A lithographic process for fabricating multi-layer semiconductor devices, comprising:
providing a substrate;
coating a first resist layer onto said substrate;
exposing said first resist layer with a mask to form a first layer exposed area and a first layer unexposed area;
depositing an opaque barrier layer on said first layer exposed area and said first layer unexposed area;

coating a second resist layer onto said opaque barrier layer;
exposing said second resist layer with a mask to form a second layer exposed area and a second layer unexposed area;
developing said second layer exposed area;
etching said opaque barrier layer;
developing said first layer exposed area; and
fabricating devices on said substrate.

Claim 19. (Original) The lithographic process according to claim 18, wherein said depositing is selected from the group consisting of: thermal evaporation, spin coating, spray coating, and electroless plating.

Claim 20. (Original) The lithographic process according to claim 18, wherein said step of coating is spun coating.